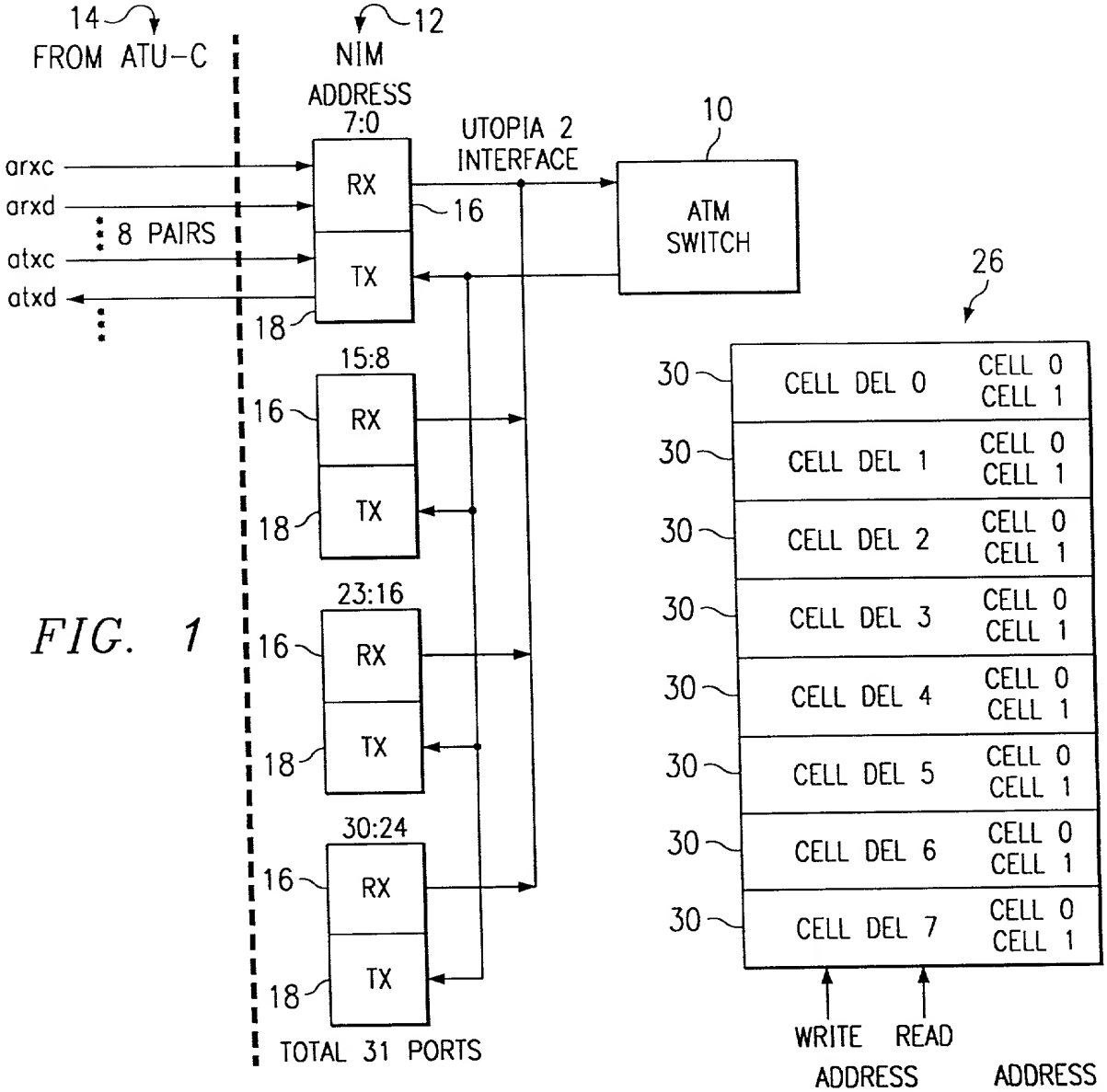


FIG. 1

FIG. 3

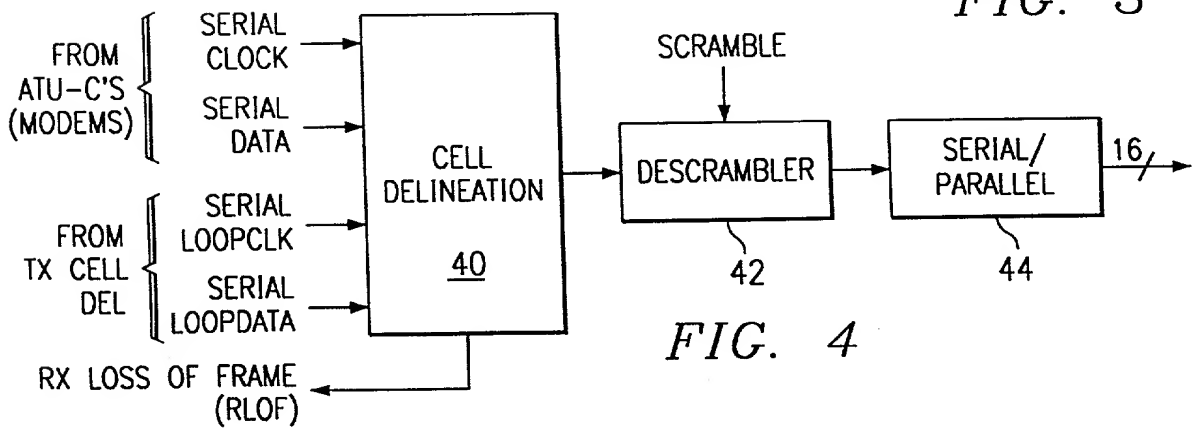
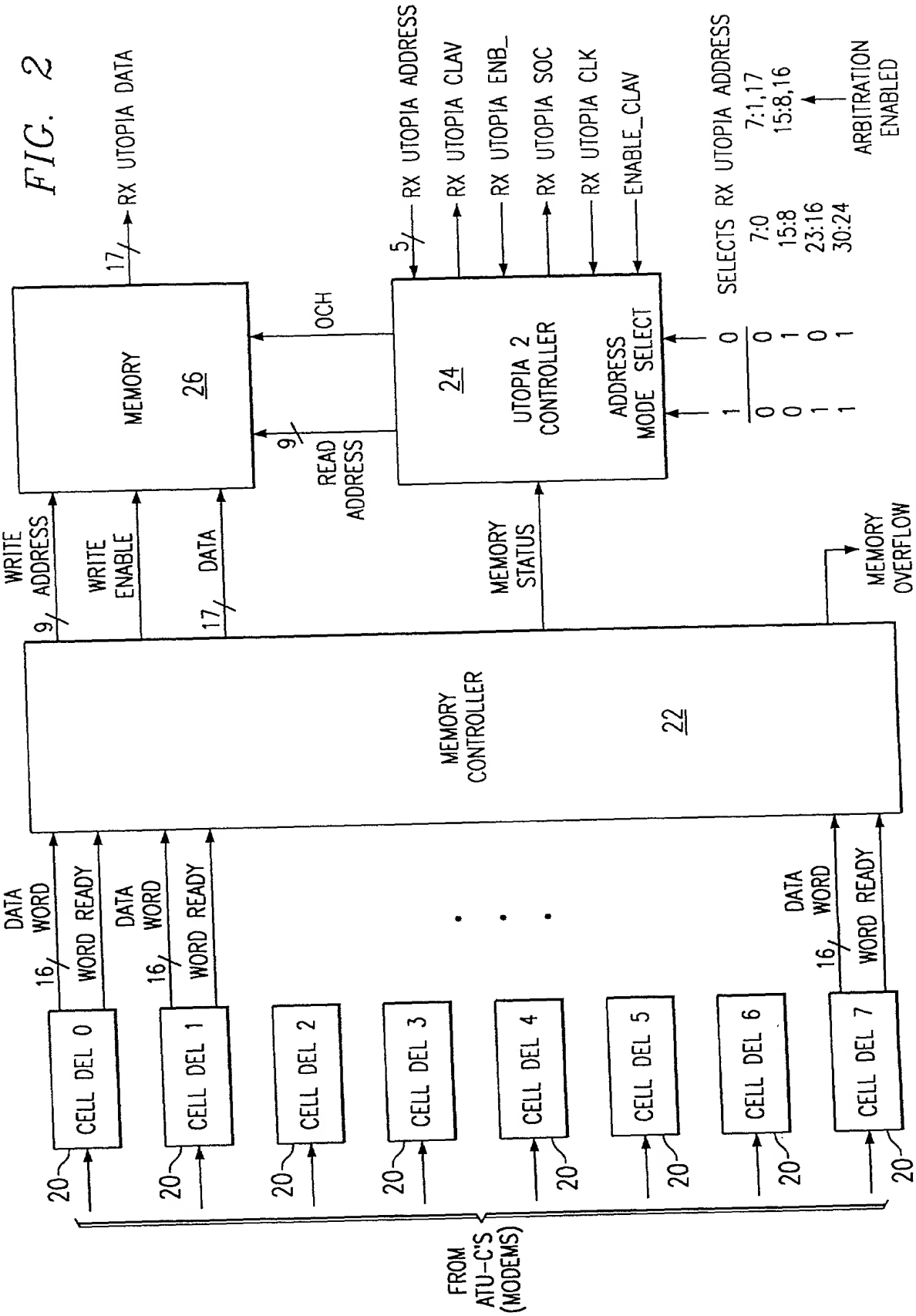
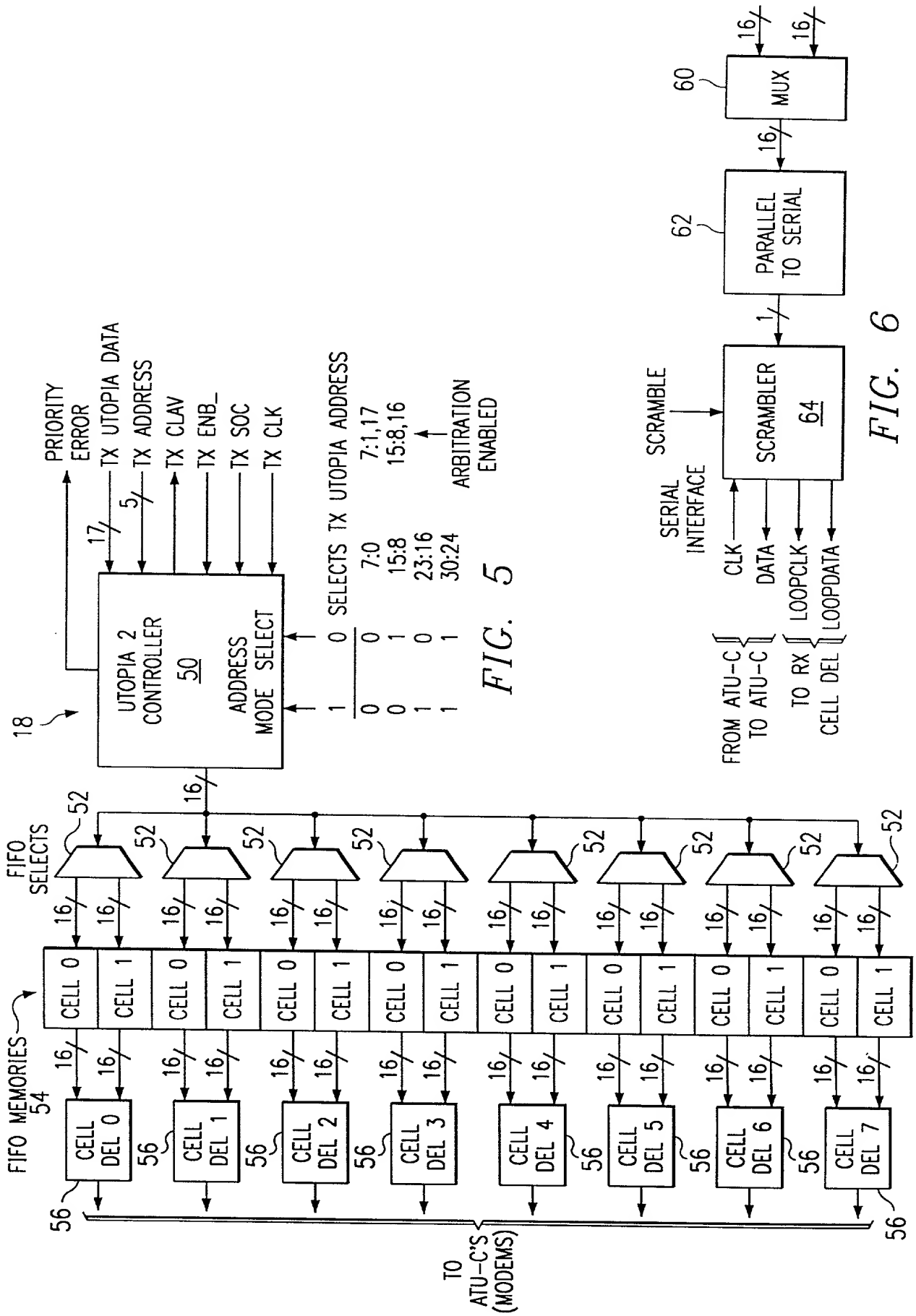


FIG. 4

FIG. 2


RX UTOPIA DATA
17
MEMORY
26
OCH
9
READ ADDRESS
5
RX UTOPIA ADDRESS
RX UTOPIA CLAV
RX UTOPIA ENB_
RX UTOPIA SOC
RX UTOPIA CLK
ENABLE_CLAV
24
UTOPIA 2 CONTROLLER
ADDRESS MODE SELECT
1 0
0 0
0 1
1 0
1 1
SELECTS RX UTOPIA ADDRESS
7:0
15:8
23:16
30:24
7:1,17
15:8,16
ARBITRATION ENABLED
WRITE ADDRESS
9
WRITE ENABLE
DATA
17
MEMORY STATUS
MEMORY OVERFLOW
MEMORY CONTROLLER
22
DATA WORD
16
WORD READY
CELL DEL 0
CELL DEL 1
CELL DEL 2
CELL DEL 3
CELL DEL 4
CELL DEL 5
CELL DEL 6
CELL DEL 7
20
FROM ATU-C'S (MODEMS)


FIFO MEMORIES 54
CELL 0
CELL 1
CELL DEL 0
CELL DEL 1
CELL DEL 2
CELL DEL 3
CELL DEL 4
CELL DEL 5
CELL DEL 6
CELL DEL 7
FIFO SELECTS
52
56
16
TO ATU-C'S (MODEMS)
18
UTOPIA 2 CONTROLLER 50
ADDRESS MODE SELECT
PRIORITY ERROR
TX UTOPIA DATA
TX ADDRESS
TX CLAV
TX ENB_
TX SOC
TX CLK
17
5
1 0 SELECTS TX UTOPIA ADDRESS
0 0 7:0
0 1 15:8
1 0 23:16
1 1 30:24
7:1,17
15:8,16
ARBITRATION ENABLED
FIG. 5
SERIAL INTERFACE
SCRAMBLE
SCRAMBLER 64
CLK
DATA
LOOPCLK
LOOPDATA
FROM ATU-C
TO ATU-C
TO RX
CELL DEL
1
PARALLEL TO SERIAL
62
MUX
60
FIG. 6